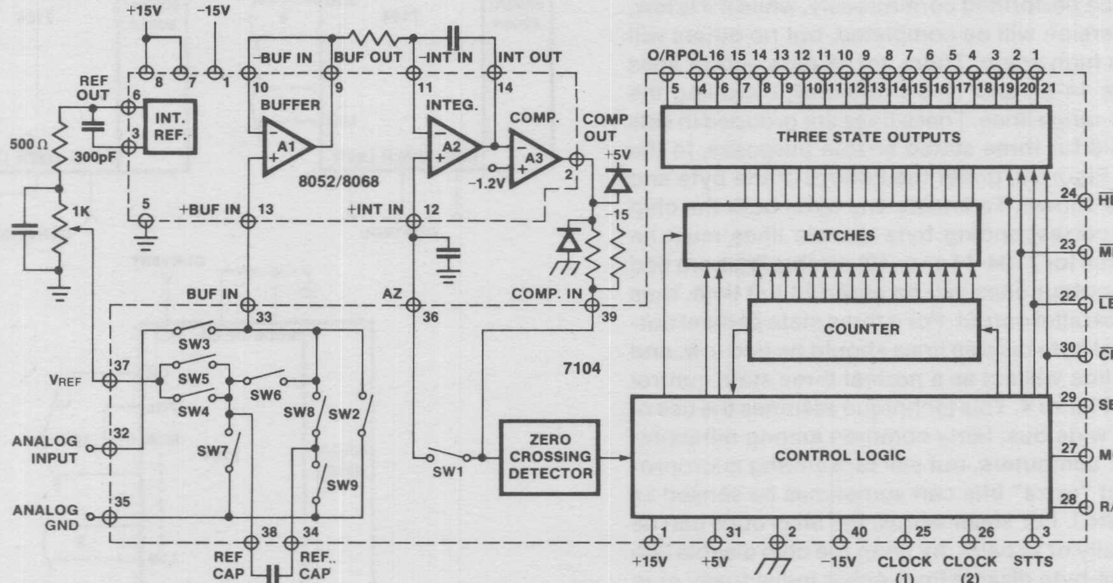
INTERSIL

The ICL7104 A Binary Output A/D Converter for μProcessors

1. INTRODUCTION

The ICL7104, combined with the ICL8052 or ICL8068, forms a member of Intersil's high performance A/D converter family. The 16-bit version, the ICL7104-16, performs the analog switching and digital function for a 16-bit binary A/D converter, with full three state output, UART handshake capability, and other outputs for a wide range of output interfacing. The ICL7104-14 and ICL7104-12 are 14 and 12-bit versions. The analog section, as with all Intersil's integrating converters, provides fully precise Auto-zero, Auto-polarity (including ± 0 null indication), single reference operation, very high input impedance, true input integration over a constant period for maximum EMI rejection, fully ratiometric operation, over-range indication, and a medium quality built-in reference. The chip pair also offers optional input buffer gain for high sensitivity applications, a built-in clock oscillator, and output signals for providing an external auto-zero capability in preconditioning circuitry, synchronizing external multiplexers, etc., etc. The basic schematic connections are shown in Figure 1.

The chip pair operates as a dual-slope integrating converter. The conversion takes place in three stages, each with their own configuration. In the first, or auto-zero phase (this is also the "idle" condition), the converter self-corrects for all the offset voltages in the buffer, integrator, and comparator. During the second, or input integrate phase, the converter integrates the input signal for a fixed time (2^{15} clock pulses for the -16 part, 2^{13} for -14, 2^{11} for -12). The converter then determines the (average) polarity of the input, and during the third, or deintegrate (alias reference integrate) phase, integrates the reference voltage in the opposite polarity, until the circuit returns to the initial condition. This point is known as the zero-crossing, and terminates the conversion process. The time (number of clock pulses) required to reach zero-crossing is proportional to the ratio of the input signal to the reference. A more detailed discussion of the operation of the dual-slope converter, including the ICL8052-ICL-710X family, is given in Application Note A017 "The Integrating A/D Converter." Figure 2 shows the basic waveforms of the Integrator.



OPTION	AZ MIN.	INTEG.	DEINTEG.
16 BIT	32K	32K	0 → 64K
14 BIT	8K	8K	0 → 16K
12 BIT	2K	2K	0 → 4K

PINS 23, 12, 13 NOT CONN. (14 BIT)
PINS 23, 10, 11, 13, 12 NOT CONN. (12 BIT)

Figure 1: 8052A (8068A)/7104 16/14/12 Bit A/D Converter.

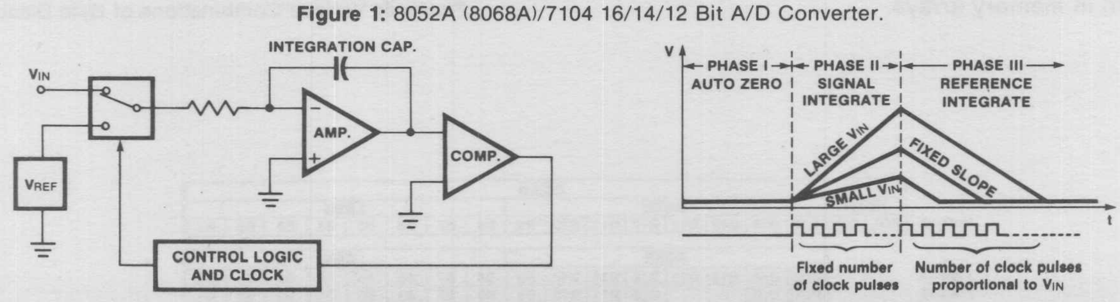


Figure 2: Simplified Dual-Slope Converter and the Three Phases of a Dual-Slope Conversion.

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This application note will first cover the digital interface of the ICL8052(ICL8068)-ICL7104 chip pair to digital systems of various kinds, including microprocessors, using the three state output capabilities (covered in Section 2) and the handshake system built into the 7104 (Section 3). Finally, some (mainly) analog techniques to enhance the system performance in certain applications are covered in Section 4. An Appendix covers a normally undetectable but under some circumstances significant error generated in the auto-zero system.

2. DIGITAL INTERFACE

(Without Internal Handshake)

The output format of the ICL7104 is extremely versatile, and includes a full internal handshake capability, which is discussed in the next section. Here we will be concerned only with the "normal" three state output lines. To disable the handshake circuitry, the MODE pin (pin 27) should be tied low (to digital gnd).

In this mode, the most useful output-timing signal is the STaTuS (STTS) line (pin 3), which goes high at the beginning of the signal integrate phase. When zero crossing occurs (or overload detection), new data is latched on the next clock pulse, and 1/2 clock pulse later, the STTS line goes low. Thus, the new data is stable on this transition. The Run/$\overline{\text{Hold}}$ pin (R/$\overline{\text{H}}$) (pin 28) is also useful for controlling conversions. A more detailed description of the operation of this pin is given in Section 4.B, but it will suffice to say here that if it is high, conversions will be performed continuously, while if it is low, the current conversion will be completed, but no others will start until it goes high again. There are 18 data output lines (16 and 14 on the 14-bit and 12-bit versions), including the polarity and over-range lines. These lines are grouped in sets of no more than 8 for three stated enable purposes, in the format shown in Figure 3, under the control of the byte and chip disable lines shown. To enable any byte, both the chip disable and the corresponding byte disable lines must be low. If all four (three for 7104-14 and -12) disable lines are tied low, all the data output lines will be asserted full time, thus giving a latched parallel output. For a three state parallel output, the three (two) byte disable lines should be tied low, and the chip disable line will act as a normal three state control line, as shown in Figure 4. This technique assumes the use of an 18 (16, 14) bit wide bus, fairly common among minicomputers and larger computers, but still rare among microprocessors (note that "extra" bits can sometimes be sensed as condition flags, etc.). For small words, the bit groups can be enabled individually or in pairs, by tying the chip disable line low, and using the byte disable lines either individually or in any combination as three state control lines, as shown in Figure 5. Several devices can be three stated to one bus by the technique suggested in Figure 6, comparable to row and column selection in memory arrays.

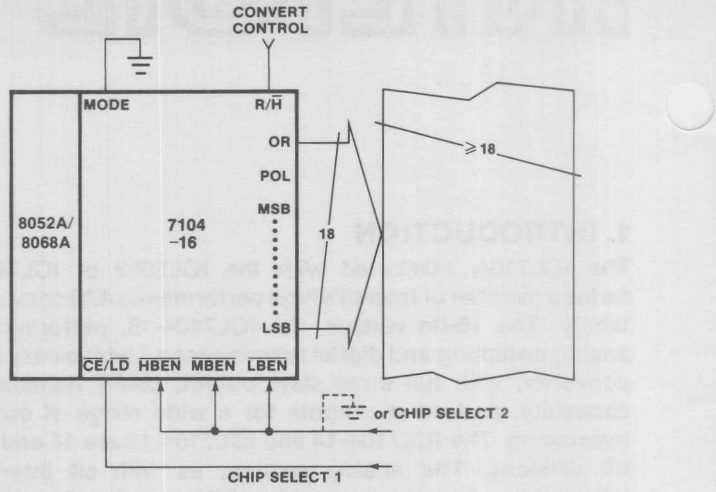

Figure 4: Full 18 Bit Three State Output

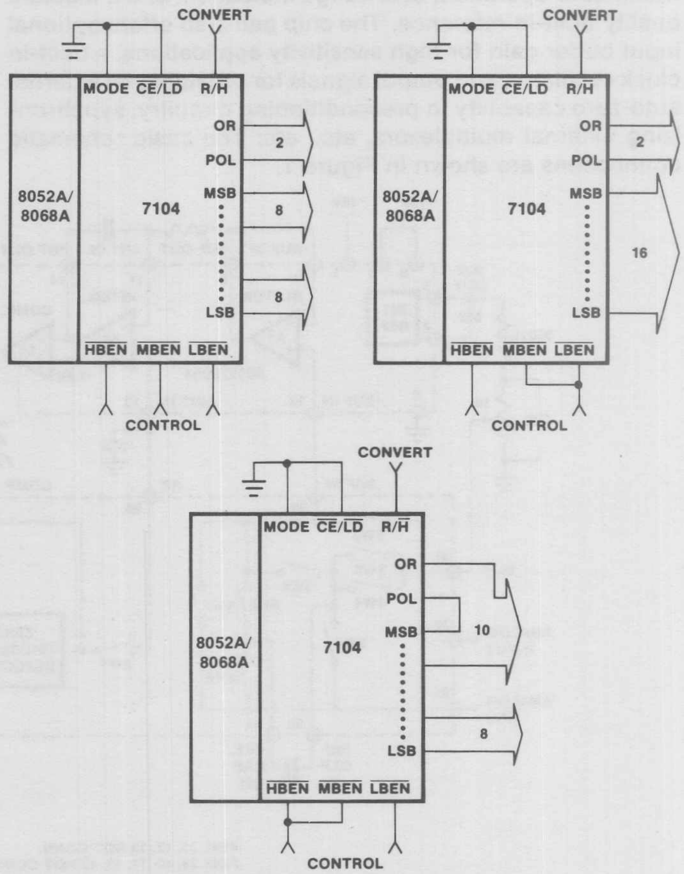

Figure 5: Various Combinations of Byte Disables

	CE/LD																	
	HBEN		MBEN								LBEN							
7104-16	POL	O/R	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1
			HBEN								LBEN							
7104-14			POL	O/R	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1
7104-12			POL	O/R			B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1
			CE/LD															

Figure 3: Three State Formats via Disable Pins

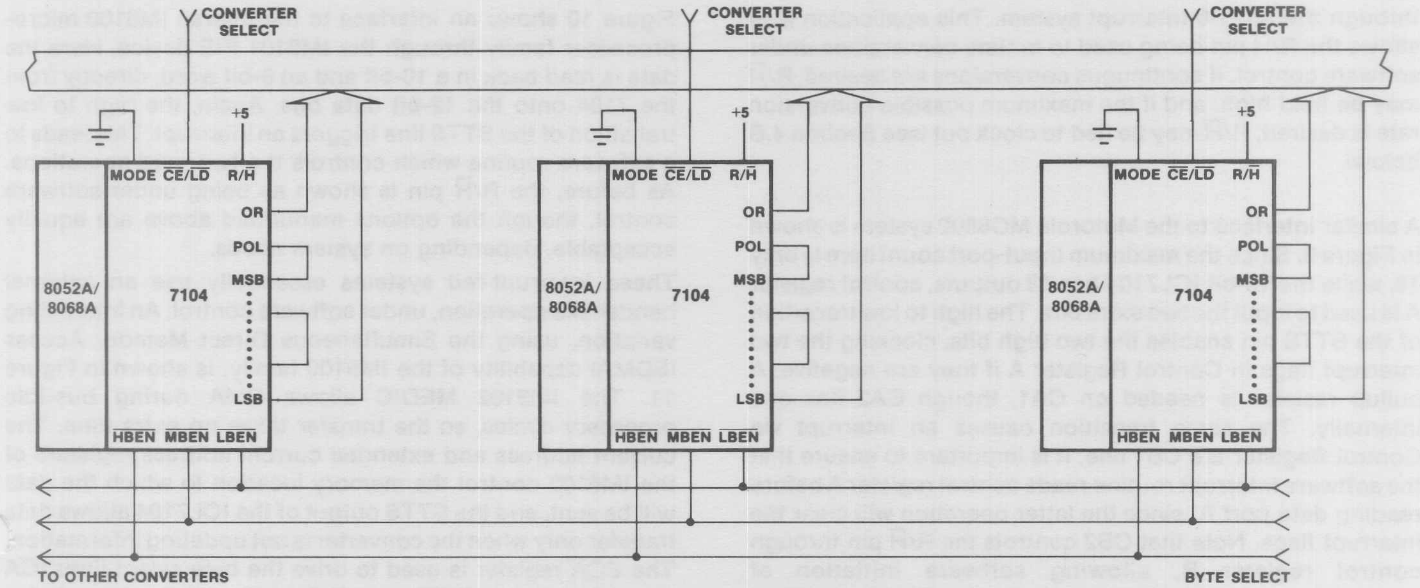

Figure 6: Three Stating Several 7104's to a Small Bus.

Some practical interface circuits utilizing the parallel and three state output capabilities of the ICL7104 are shown in Figures 7 through 13. Figure 7 shows a straightforward application to the Intel MCS-48, 80, and 85 systems via an 8255 PPI, using full-time parallel output. The I/O ports of an 8155 can be used in the same way. This interface can be used in a read-anytime mode, although there can be timing problems here, since a read performed as new data is being latched in the ICL7104 may lead to scrambled data. (Note that this will occur only very rarely, in proportion to the ratio of setup-skew to conversion times). One way to overcome this problem is to read back the STTS line as well, and if it is high, read the data again after a delay exceeding 1/2 (converter) clock cycle. If STTS is now low, the second reading is correct, if it is still high, the first reading was correct (note that data never changes when STTS is low, and it goes low 1/2 clock cycle after data update occurs). Alternatively, the problem is completely avoided by using a read-after-update mode, as shown in Figure 8. Here the high to low transition of STTS triggers a "read data" operation

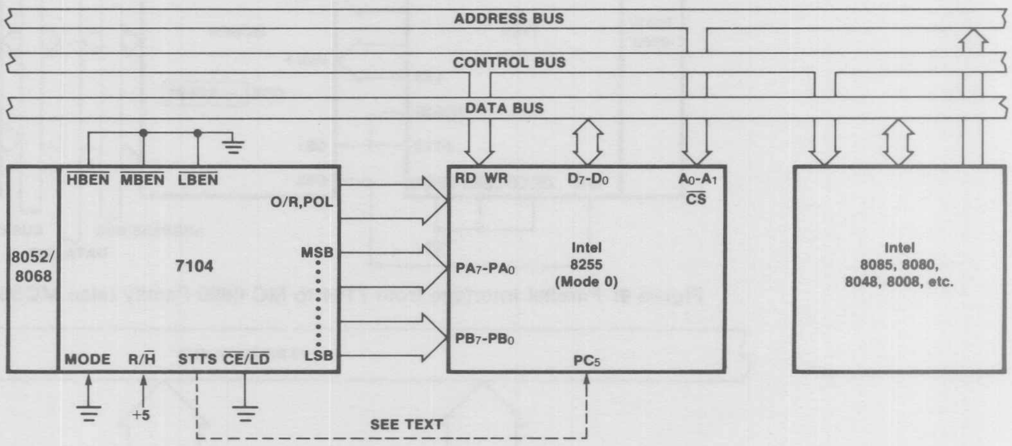

Figure 7: Full Time Parallel/Interface 8052(8068)-7104 to MCS-48, 80/85 Families

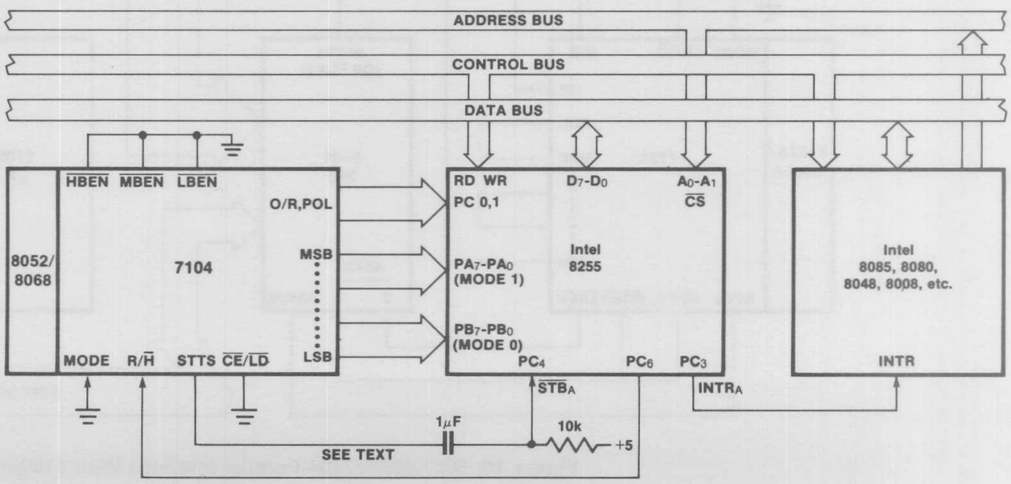

Figure 8: Full Time Parallel Interface 8052(8068)-7104 to MCS-48, 80/85 Families With Interrupt

through the MCS-8 Interrupt system. This application also shows the R/$\overline{H}$ pin being used to initiate conversions under software control. If continuous conversions are desired, R/$\overline{H}$ may be held high, and if the maximum possible conversion rate is desired, R/$\overline{H}$ may be tied to clock out (see Section 4.B below).

A similar interface to the Motorola MC6800 system is shown in Figure 9. Since the maximum input-port count here is only 16, while the 16-bit ICL7104 has 18 outputs, control register A is used to input the two extra bits. The high to low transition of the STTS pin enables the two high bits, clocking the two interrupt flags in Control Register A if they are negative. A pullup resistor is needed on CA1, though CA2 has one internally. The same transition causes an interrupt via Control Register B's CB1 line. It is important to ensure that the software interrupt routine reads control register A before reading data port A, since the latter operation will clear the interrupt flags. Note that CB2 controls the R/$\overline{H}$ pin through control register B, allowing software initiation of conversions in this system also. Naturally, the 14 and 12 bit versions of the ICL7104 avoid this problem since 16 or fewer bits need to be read back. Since the MOS Technology MCS650X microprocessors are bus-compatible with the MC6800's the same circuit can be used with them also.

Figure 10 shows an interface to the Intersil IM6100 microprocessor family through the IM6101 PIE device. Here the data is read back in a 10-bit and an 8-bit word, directly from the 7104 onto the 12-bit data bus. Again, the high to low transition of the STTS line triggers an interrupt. This leads to a software routine which controls the two read operations. As before, the R/$\overline{H}$ pin is shown as being under software control, though the options mentioned above are equally acceptable, depending on system needs.

These Interrupt-fed systems essentially use an external handshake operation, under software control. An interesting variation, using the Simultaneous Direct Memory Access (SDMA) capability of the IM6100 family, is shown in Figure 11. The IM6102 MEDIC allows DMA during bus-idle processor cycles, so the transfer takes no extra time. The current address and extended current address registers of the IM6102 control the memory location to which the data will be sent, and the STTS output of the ICL7104 allows data transfer only when the converter is not updating information. The ECA register is used to drive the byte select lines (CA should be set to 7777, and WC to 2) and the User Pulse controls Chip disable $\overline{CE}/\overline{LD}$. A more fully loaded system can use address latches for CA. A DMA system can also be set up on the MCS-8 system using the DMA controller, 8257, and the three state outputs of the ICL7104.

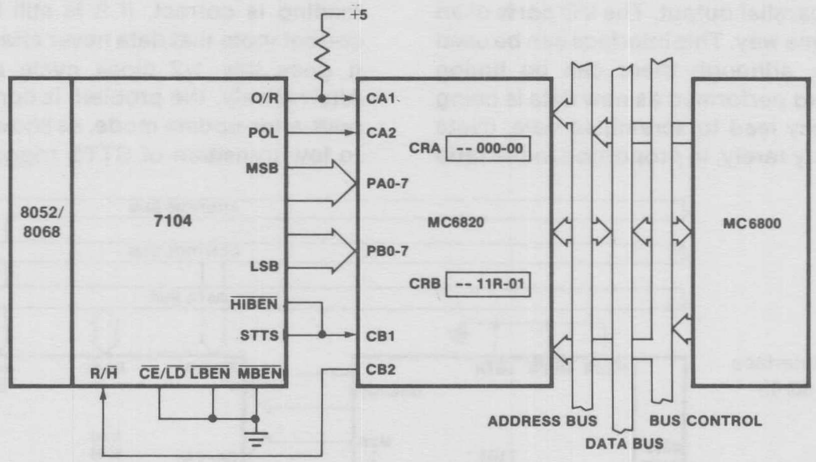

Figure 9: Parallel Interface from 7104 to MC 6800 Family (also MCS650X Family)

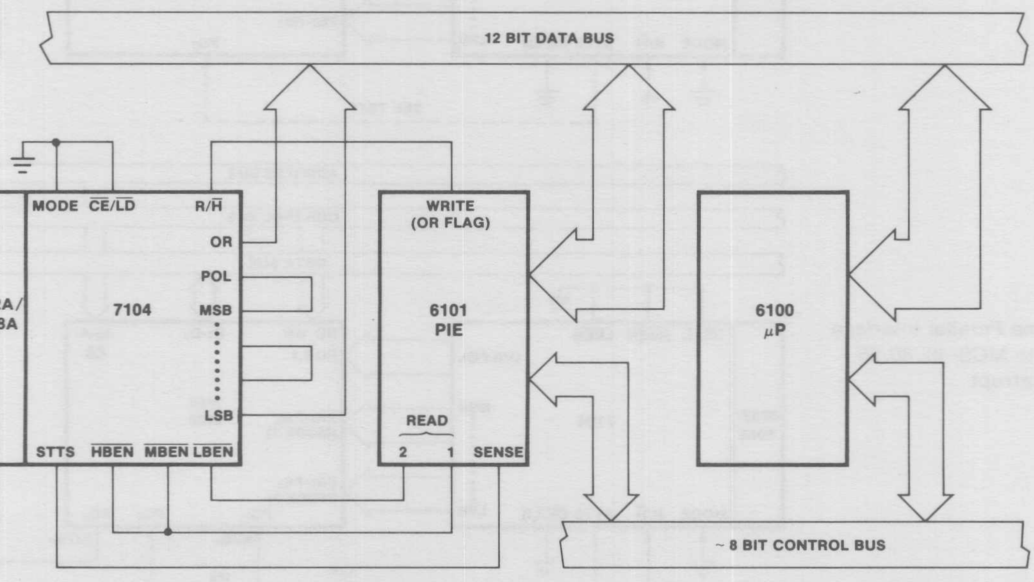

Figure 10: 8052(8068)/7104 Parallel Interface With 6100μP

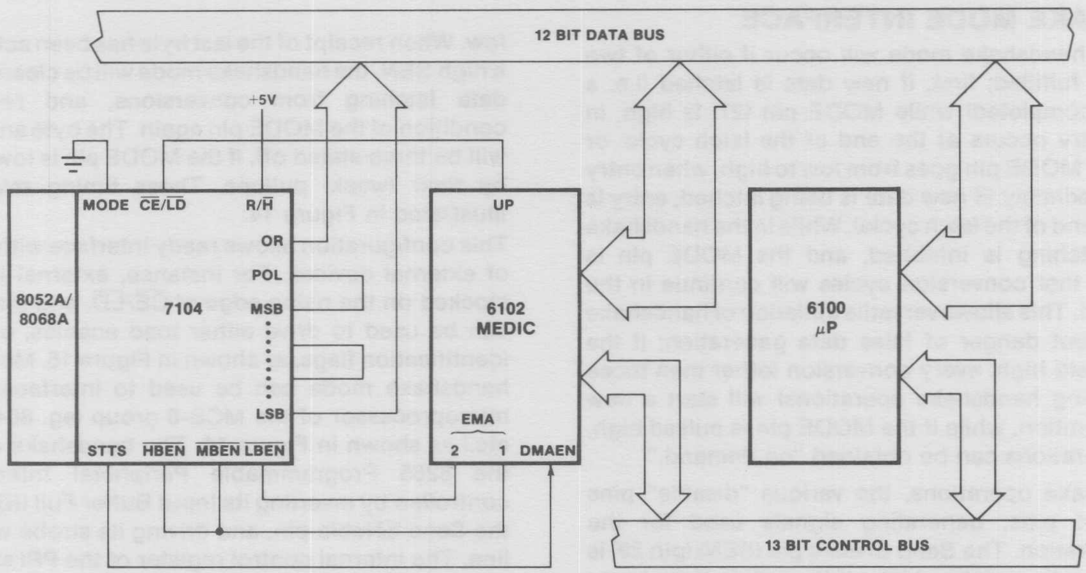

Figure 11: 8052(8068)/7104 Parallel Interface With 6100µP Using DMA

It is possible using the three state output capability, to connect the ICL7104 directly onto many microprocessor busses. Examples of this are shown in Figures 12 and 13. It is necessary to consider the system timing in this kind of application, and careful study should be made of the required set-up times from the microprocessor data sheets.

Note also the drive limitations on long busses. Generally this type of circuit is only favored if the memory peripheral address density is low, so that simple redundant address decoding can be used. Interrupt handling can require multiple external components also, and use of an interface device is normally advisable if this is needed.

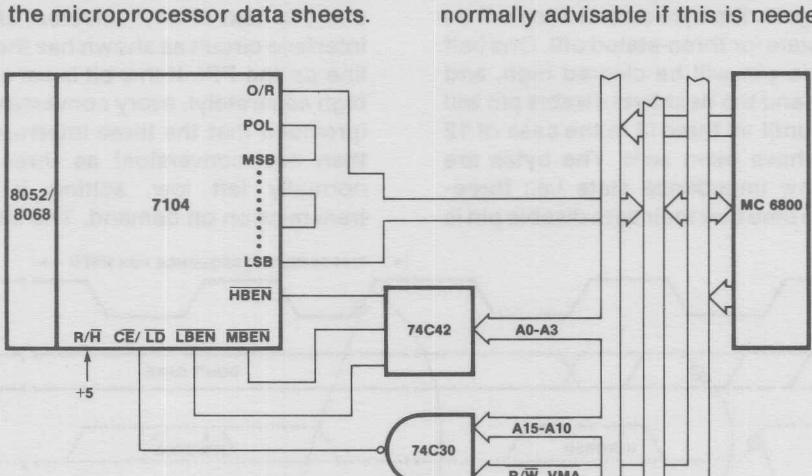

Figure 12: Direct 8052(8068)/7104 to MC6800 Microprocessor Interface

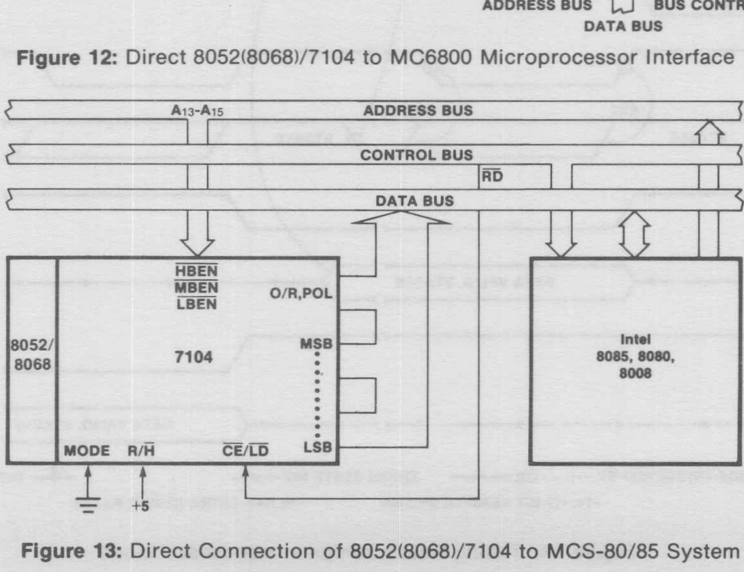

Figure 13: Direct Connection of 8052(8068)/7104 to MCS-80/85 System

3. HANDSHAKE MODE INTERFACE

Entry into the handshake mode will occur if either of two conditions are fulfilled; first, if new data is latched (i.e. a conversion is completed) while MODE pin (27) is high, in which case entry occurs at the end of the latch cycle; or secondly, if the MODE pin goes from low to high, when entry will occur immediately (if new data is being latched, entry is delayed to the end of the latch cycle). While in the handshake mode, data latching is inhibited, and the MODE pin is ignored. (Note that conversion cycles will continue in the normal manner). This allows versatile initiation of handshake operation without danger of false data generation; if the MODE pin is held high, every conversion (other than those completed during handshake operations) will start a new handshake operation, while if the MODE pin is pulsed high, handshake operations can be obtained "on demand."

During handshake operations, the various "disable" pins become output pins, generating signals used for the handshake operation. The Send ENable pin (SEN) (pin 29) is used as an indication of the ability of the external device to receive data. The condition of the line is sensed once every clock pulse, and if it is high, the next (or first) byte is enabled on the next rising CL1 (pin 25) clock edge, the corresponding byte disable line goes low, and the $\overline{\text{C}}$hip Disabl$\overline{\text{E}}$/$\overline{\text{L}}$oa$\overline{\text{D}}$ line (pin 30) ($\overline{\text{CE}}/\overline{\text{LD}}$) goes low for one full clock pulse only, returning high.

On the next falling CL1 clock pulse edge, if SEN remains high, or after it goes high again, the byte output lines will be put in the high impedance state (or three-stated off). One half pulse later, the byte disable pin will be cleared high, and (unless finished) the $\overline{\text{CE}}/\overline{\text{LD}}$ and the next byte disable pin will go low. This will continue until all three (2 in the case of 12 and 14 bit devices) bytes have been sent. The bytes are individually put into the low impedance state i.e.: three-stated on during most of the time that their byte disable pin is low. When receipt of the last byte has been acknowledged by a high SEN, the handshake mode will be cleared, re-enabling data latching from conversions, and recognizing the condition of the MODE pin again. The byte and chip disables will be three stated off, if the MODE pin is low, but held high by their (weak) pullups. These timing relationships are illustrated in Figure 14.

This configuration allows ready interface with a wide variety of external devices. For instance, external latches can be clocked on the rising edge of $\overline{\text{CE}}/\overline{\text{LD}}$, and the byte disables can be used to drive either load enables, or provide data identification flags, as shown in Figure 15. More usefully, the handshake mode can be used to interface with an 8-bit microprocessor of the MCS-8 group (eg. 8048, 8080, 8085, etc.) as shown in Figure 16. The handshake operation with the 8255 Programmable Peripheral Interface (PPI) is controlled by inverting its Input Buffer Full (IBF) flag to drive the Send ENable pin, and driving its strobe with the $\overline{\text{CE}}/\overline{\text{LD}}$ line. The internal control register of the PPI should be set in mode 1 for the port used. If the 7104 is in handshake mode, and the 8255 IBF flag is low, the next word will be presented to the chosen port, and strobed. The strobe will cause IBF to rise, locking the three stated byte on. The PPI will cause a program interrupt in the MCS-8 system, which will result (after the appropriate program steps have been executed) in a "read" operation. The byte will be read, and the IBF reset low. This will cause the current byte disable to be dropped, and the next (if any) selected, strobed, etc., as before. The interface circuit as shown has the MODE pin tied to a control line on the PPI. If this bit is set always high (or mode is tied high separately), every conversion will be fed into the system (provided that the three interrupt sequences take less time than one conversion) as three 8-bit bytes; if this bit is normally left low, setting it high will cause a data transmission on demand. The interrupt routine can be used

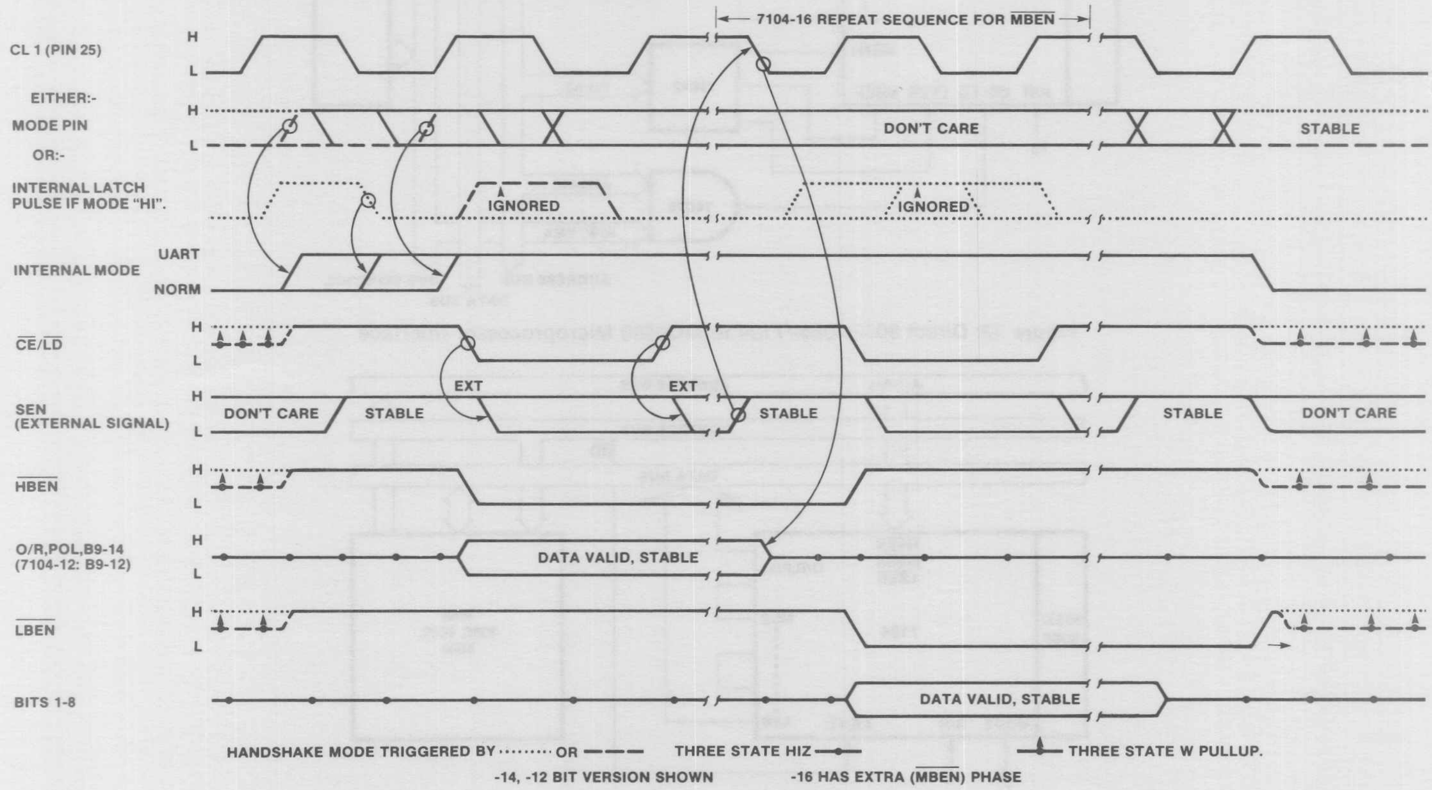

Figure 14: Timing Relationships in Handshake Mode

to reset the bit, if desired. Note also that the R/$\overline{H}$ pin is also shown tied to a control bit so that conversions can be performed either continuously or on demand under software control. Note that one port is not used here, and can service another peripheral device. The same arrangement can again be used with an 8155 I/O port and control lines.

Similar methods can be used with other microprocessors, such as the MC6800 or MCS650X family, as shown in Figure 17, and the Intel MCS4/40 family, as shown in Figure 18. These both operate almost identically to the method described above, except that in the former both R/$\overline{H}$ and MODE are shown tied high, to avoid using a full port for only two lines. Any 8-bit or wider microprocessor (or mini-computer), or narrower devices with 8-bit wide ports (most 4-bit devices have 8-bit wide ports available) can be interfaced in a handshake mode with a minimum of additional hardware, frequently none at all.

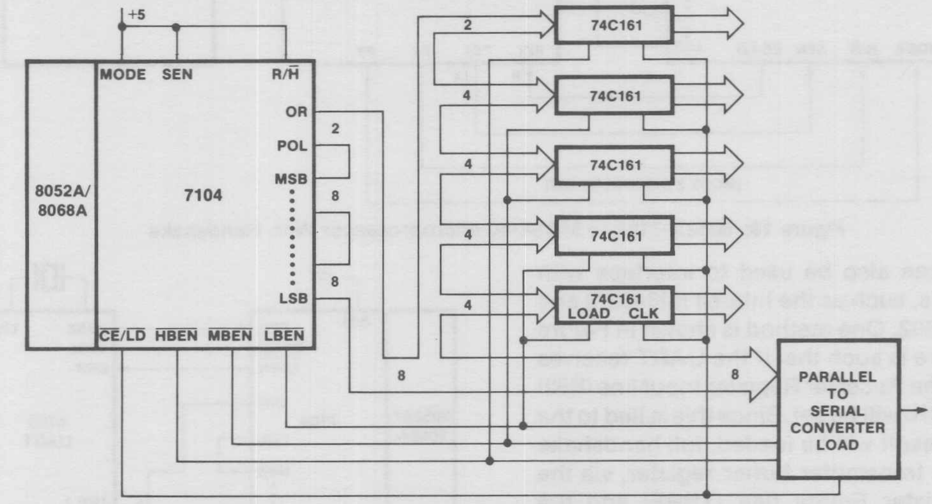

Figure 15: Use of Byte Disable Lines as Flags or for Loading

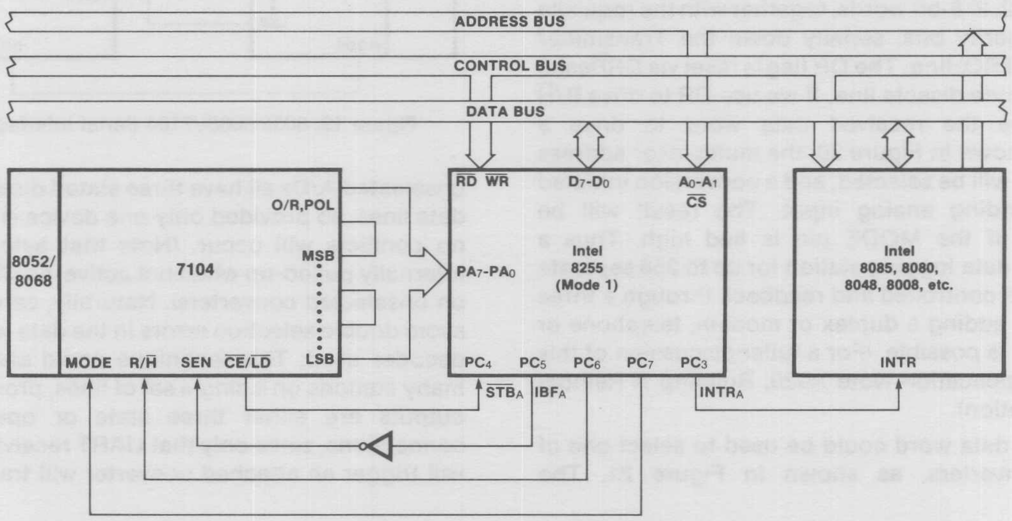

Figure 16: 8052A(8068A)-7104 to MCS-48, -80, or -85 Handshake Interface

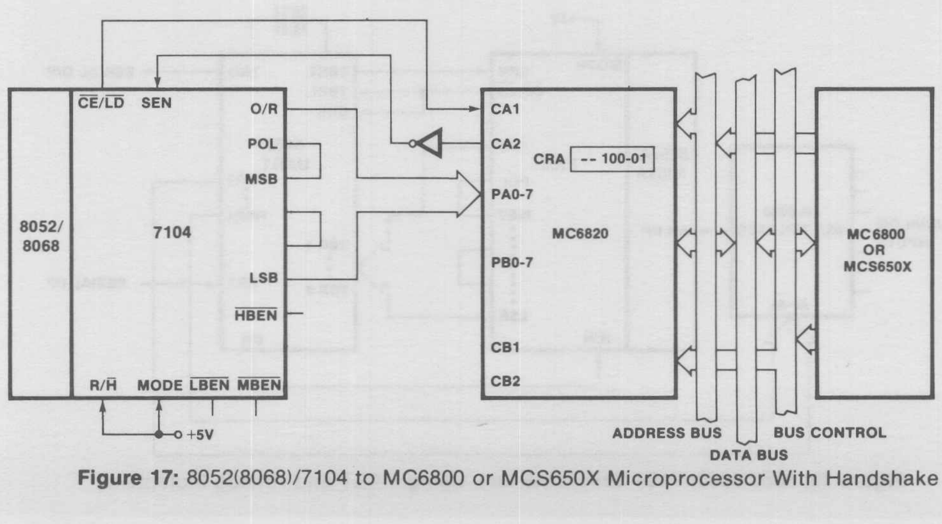

Figure 17: 8052(8068)/7104 to MC6800 or MCS650X Microprocessor With Handshake

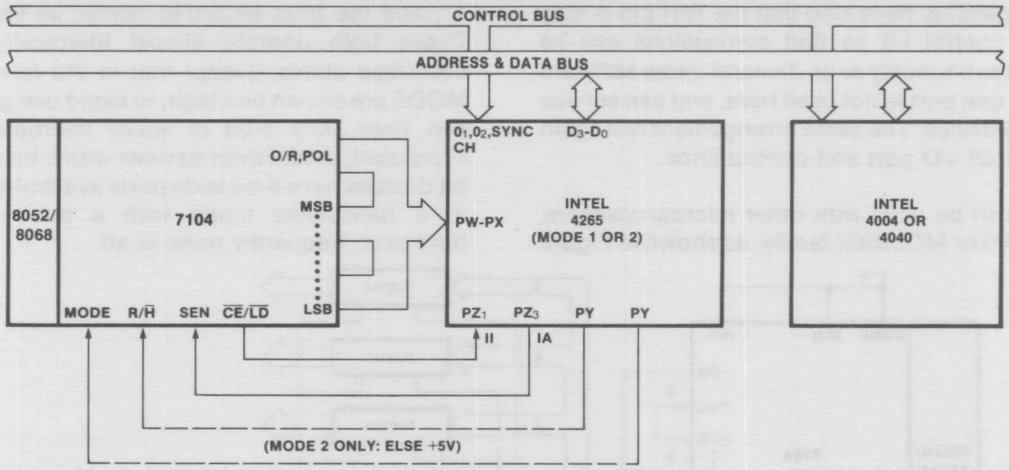

Figure 18: 8052A-7104 to MCS4/40 Microprocessor With Handshake

The handshake mode can also be used to interface with industry-standard UARTs, such as the Intersil IM6402/3 and the Western Digital TR1602. One method is shown in Figure 19. The arrangement here is such that if the UART receives any word serially down the Receiver Register Input line (RRI) the Data Received flag (DR) will be set. Since this is tied to the MODE pin, the current result will be loaded, full handshake style as before, into the transmitter buffer register, via the Transmitter Buffer Register Empty flag (TBRE) and the TBRLoad lines. The UART will thus transmit the full 18 (16, 14) bit result in 3 (2, 2) 8-bit words, together with the requisite start, stop and parity bits, serially down the Transmitter Register Output (TRO) line. The DR flag is reset via DRReset, here driven by a byte disable line. If we use DR to drive R/$\overline{H}$ instead, and use the received data word to drive a multiplexer, as shown in Figure 20, the multiplexer address sent to the UART will be selected, and a conversion initiated of the corresponding analog input. The result will be returned serially if the MODE pin is tied high. Thus a complete remote data logging station for up to 256 separate input lines can be controlled and readback through a three line interface. By adding a duplex or modem, telephone or radio link control is possible. (For a fuller discussion of this technique, see Application Note A025, Building A Remote Data Logging Station).

Alternatively, the data word could be used to select one of several A/D converters, as shown in Figure 21. The unselected A/Ds all have three stated disable lines as well as data lines, so provided only one device is selected at a time, no conflicts will occur. (Note that byte disable lines are internally pulled-up when not active, so $\overline{CE}/\overline{LD}$ has no effect on unselected converters). Naturally, care must be taken to avoid double selection errors in the data word, or an address decoder used. This technique could also be used to poll many stations on a single set of lines, provided that the TRO outputs are either three state or open collector/drain connections, since only that UART receiving an address that will trigger an attached converter will transmit anything.

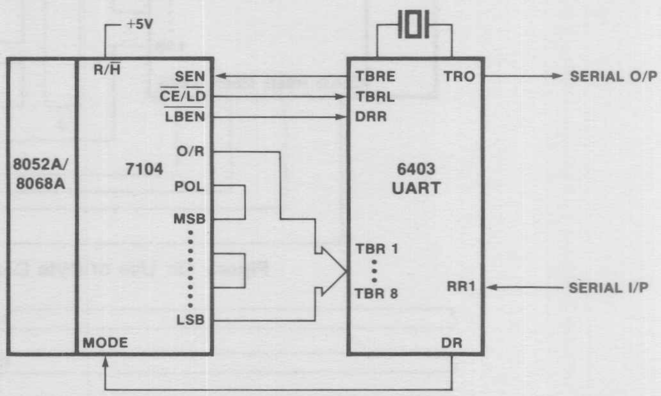

Figure 19: 8052(8068)/7104 Serial Inferface Using UART

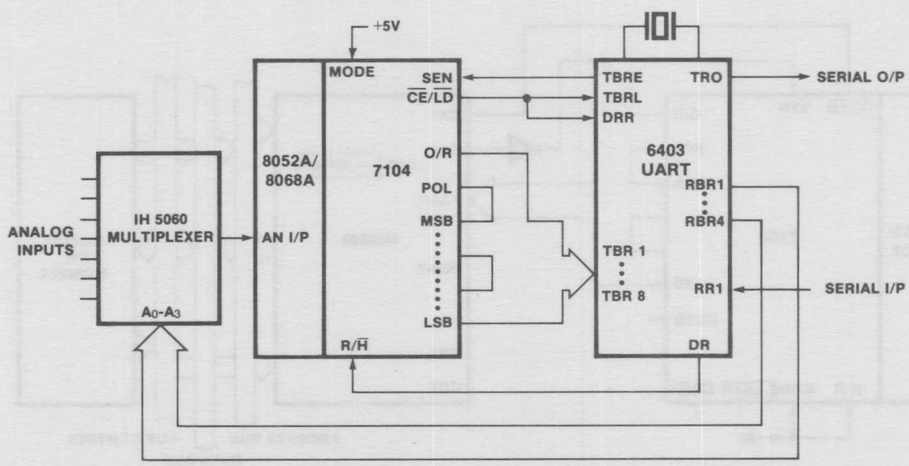

Figure 20: 8052(8068)/7104 Serial Interface Using UART and Analog Multiplexer

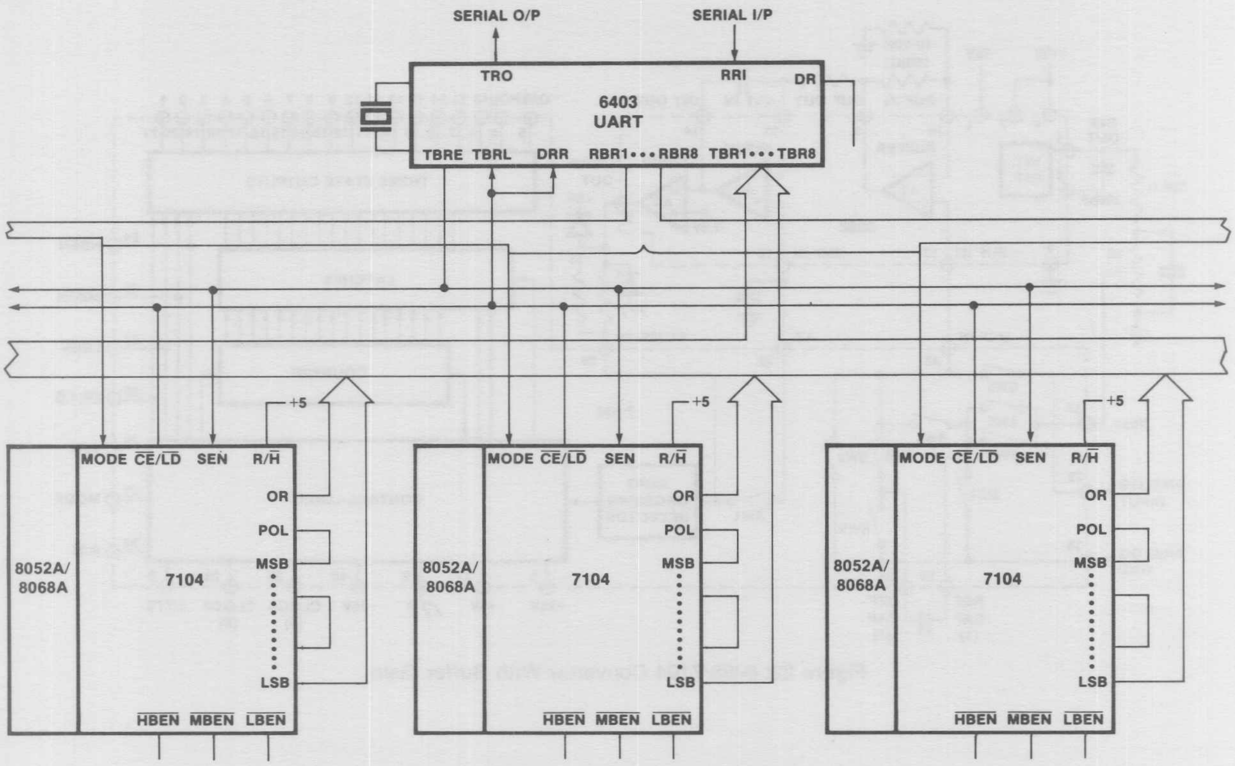

Figure 21: Multiplexing Converters Through the Mode Pin

4. MISCELLANEOUS TECHNIQUES FOR PERFORMANCE ENHANCEMENT

This section covers a few techniques, primarily analog, that can be used to enhance the performance of the ICL8052 (ICL8068)/ICL7104 chip pair for certain applications. Section 4.A. deals with buffer gain, for sensitivity increases of up to about 5 or 10 to 1, Section 4.B. with a special interconnection to allow the maximum rate of conversion with lower-valued inputs, and Section 4.C. external auto-zero for extending the benefits of auto-zero operation to preamplifiers, etc., to cover specialized signal processing or sensitivity enhancement by 10-100 to 1.

4.A. Buffer Gain

One of the significant contributions to the effective input noise voltage of a dual slope integrator is the so called auto-zero noise. At the end of the auto-zero interval, the instantaneous noise voltage on the auto-zero capacitor is stored, and subtracts from the input voltage while adding to the reference voltage during the next cycle. Although the open loop band width of the auto-zero loop is not wide, the gain from the input is very high, and the resulting closed loop band width to buffer noise is fairly wide. The result is that this noise voltage effectively is somewhat greater than the input noise voltage of the buffer itself during integration. By introducing some voltage gain into the buffer, the effect of the auto-zero noise (referred to the input) can be reduced to the level of the inherent buffer noise. This generally occurs with a buffer gain of between 3 and 10. Further increase in buffer gain merely increases the total offset to be handled by the auto-zero loop, and reduces the available buffer and integrator swings, without improving the noise performance of the system (see also the appendix). The circuit recommended for doing this with the ICL8068/ICL7104 is shown in Figure 22. With careful layout, the circuit shown can achieve effective input noise voltages on the order of 1-2μV, allowing full 16-bit use with full scale inputs of as low as 150mV. Note that at this level, thermoelectric EMFs between PC boards, IC pins, etc., due to local temperature changes can be very troublesome. Considerable care has been taken with the internal design of the ICL7104 and the ICL8068 to minimize the internal thermoelectric effects, but device dissipation should be minimized, and the effects of heat from adjacent (and not-so adjacent) components must be considered to achieve full performance at this sensitivity level.

4.B. Minimal Auto-Zero Time Operation

The R/$\overline{H}$ pin (pin 28) can be used in two basic modes. If it is held high, the ICL7104-16 will perform a complete conversion cycle in 131K clock counts (strictly 2^{17}), regardless of the result value (for the -14, 2^{15} counts, -12, 2^{13} counts).

If, however, the R/$\overline{H}$ pin (ever) goes low between the time of the zero-crossing and the end of a full $2^{16/14/12}$ count reference integrate phase, that phase is immediately terminated. If it is then held low, the 7104 will ensure a minimum auto-zero count (of $2^{15/13/11}$ counts) and then wait in auto-zero until the R/$\overline{H}$ pin goes high. On the other hand, if it goes high immediately subsequent to this minimal auto-zero count, the 7104 will start the next conversion after the least permissible time in auto-zero; i.e., at the maximum possible rate. The necessary "activity" on the R/$\overline{H}$ pin can be readily provided by tying it to the clock out pin (pin 26). Obviously under these conditions, the conversion cycle time depends on the result. Also note the scale factor and auto-zero effects covered in the Appendix.

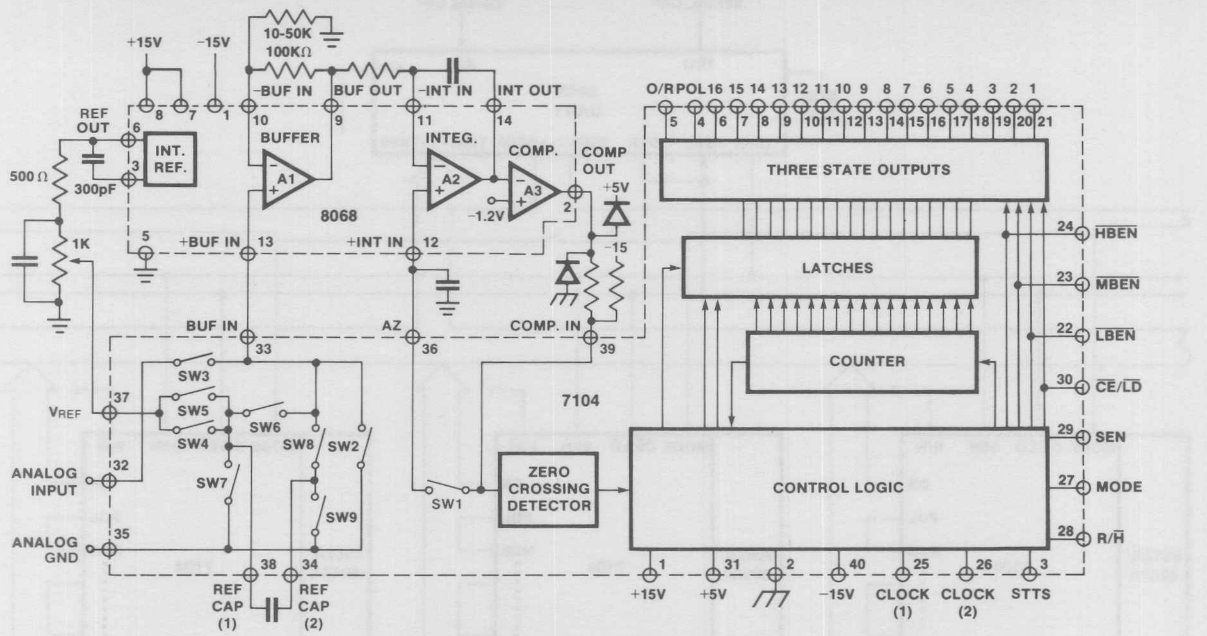

Figure 22: 8068/7104 Converter With Buffer Gain

4. C. External Auto-Zero

In many systems, signal conditioning is required in front of the converter for preamplification, filtering, etc., etc. With the exception of buffer gain, discussed in Section 4.A. above, it is generally not possible to include these conditioning circuits in the auto-zero loop. However, a sample-and-difference circuit keyed to the auto-zero phase can be used to eliminate offset and similar errors in preamplifiers, multiplexers, etc. A suitable circuit for a simple system is shown in Figure 23. The ICL8053 is used as a switch here primarily because of its extremely low charge injection (typically well below 10pC), even though it does limit the analog swing to ±4V. The use of an IH191 or IH5043 avoids this restriction, but increases the charge injection. The circuit of Figure 24 includes some balancing, but still injects typically 60pC (or 150pC for a DG191). Note that all these circuits have some sensitivity to stray capacitance at the converter input node. The amplifying or conditioning stages indicated in both these circuits must be capable of passing the chopping frequency with small enough delay, rise time, and overshoot to lead to insignificant error. Filtering should be done before or after the switching devices. Note also that although the input signal is still integrated over the normal time period, the input reference level is not. The time constant of the hold capacitor charging circuit should take noise and interference effects into consideration.

For a multiplexed input system, an arrangement similar to that of Figure 25 may be needed with individual preconditioning amplifiers, and Figure 26 with a common preconditioning amplifer. Note that in both of these cases, the capacitor may be charged to different voltages on each channel. By putting a capacitor in each line of Figure 25, the capacitor charging transients are eliminated, but the multiplexer capacitance becomes an important source of stray capacitance.

5. SUMMARY

The list of applications presented here is not intended to be, nor can it be, exhaustive, but is intended to suggest the wide range of possible applications of the ICL8052(ICL8068)/ICL7104 chip pair in A/D conversion in a digital environment. Many of the ideas suggested here may be used in combination; in particular, all the digital concepts discussed in Sections 2 and 3 can be used with any of the analog techniques outlined in Section 4, and many of the uses of the R/$\overline{H}$ and MODE pins can be mixed.

Some other applications bulletins that may be found useful are listed here:

A016 "Selecting A/D Converters", by Dave Fullagar

A017 "The Integrating A/D Converter", by Lee Evans

A018 "Do's and Dont's of Applying A/D Converters", by Peter Bradshaw and Skip Osgood

A025 "Building a Remote Data Logging Station", by Peter Bradshaw

R005 "Interfacing Data Converters & Microprocessors", by Peter Bradshaw et al, Electronics, Dec. 9, 1976.

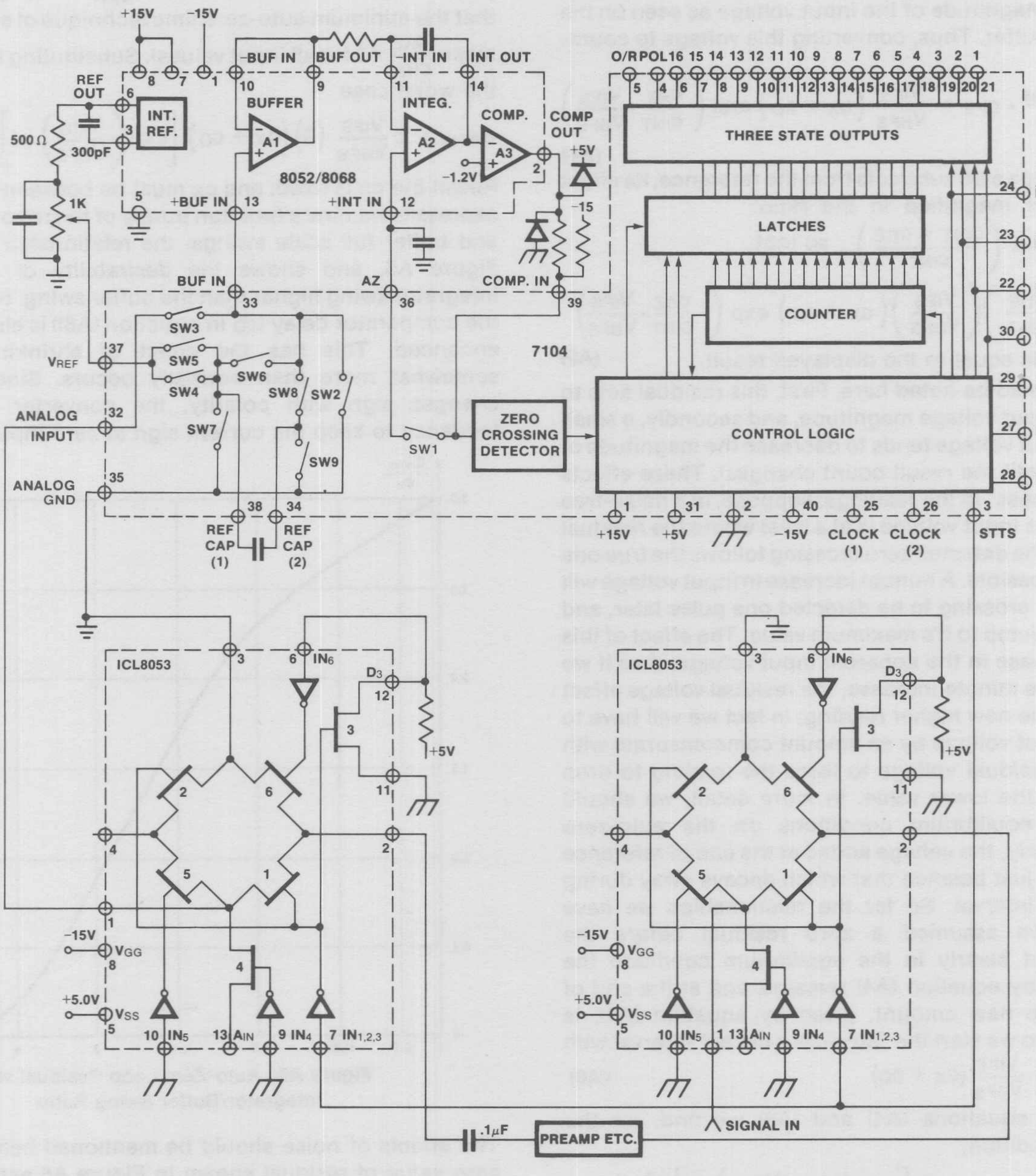

Figure 23: External Auto-Zero System Using 8053 Switches

Now $R_{INT}C_{INT}$ is controlled by the buffer swing, V_{BFS}, the integrator swing, V_{IFS}, and the integration time $t_{INT} = c_{INT}\,t_{cp}$, so that

$$V_{BFS}/R_{INT} \cdot t_{INT} = C_{INT}\,V_{IFS}, \text{ or } R_{INT}\,C_{INT} = c_{INT}\frac{V_{BFS}}{V_{IFS}}\,t_{cp}$$

and

$$V_{AZres} = V_{Ires}\left(\exp - \frac{c_{AZ}V_{IFS}}{c_{INT}V_{BFS}}\right) \tag{A3}$$

This residual voltage on the auto-zero capacitor effectively increases the magnitude of the input voltage as seen on the output of the buffer. Thus, converting this voltage to count-equivalents,

$$c_{AZres} = \frac{V_{AZres}}{V_{BFS}} \cdot c_{FS} = \frac{V_{IFS}}{V_{BFS}}\left(c_X + c_D\right)\exp\left(-\frac{c_{AZ}}{c_{INT}}\cdot\frac{V_{IFS}}{V_{BFS}}\right) \tag{A4}$$

Since this voltage also subtracts from the reference, its effect at the input is magnified in the ratio

$$c_{INres} = c_{AZres}\left(\frac{c_{INT} + c_{DE}}{c_{INT}}\right), \text{ so that}$$

$$c_{INres} = \left(1 + \frac{c_{DE}}{c_{INT}}\right)\left(\frac{V_{IFS}}{V_{BFS}}\right)\left(c_X + c_D\right)\exp\left(-\frac{c_{AZ}}{c_{INT}}\cdot\frac{V_{IFS}}{V_{BFS}}\right) \tag{A5}$$

Note that c_{DE} is equal to the displayed result.

Two things should be noted here. First, this residual acts to increase the input voltage magnitude, and secondly, a small increase in input voltage tends to decrease the magnitude of the residual (until the result count changes). These effects lead to "stickyness" in the readings; suppose, in a noise-free system, that the input voltage is at a level where the residual is a minimum; the detected zero crossing follows the true one as closely as possible. A minute increase in input voltage will cause the zero crossing to be detected one pulse later, and the residual to jump to it's maximum value. The effect of this is a small increase in the apparent input voltage; thus if we now remove the minute increase, the residual voltage effect will maintain the new higher reading; in fact we will have to reduce the input voltage by an amount commensurate with the effective residual voltage to force the reading to drop back again to the lower value. In more detail, we should consider the equilibrium conditions on the auto-zero capacitor. Clearly, the voltage added at the end of reference integrate must just balance that which decays away during the auto-zero interval. So far the relationships we have developed have assumed a zero residual before the conversion, but clearly in the equilibrium condition the residual given by equation (A4) remains, and at the end of conversion, the new amount, given by equation (A1), is added to this, so we start the "auto-zero decay" interval with

$$c_{Ires} = c_{AZres} + \frac{V_{IFS}}{V_{BFS}}\left(c_X + c_D\right) \tag{A6}$$

By combining equations (A4) and (A6) we find, for the equilibrium condition,

$$c_{AZres} = \pm\frac{V_{IFS}}{V_{BFS}}\left(c_X + c_D\right)\left[\exp\left\{+\frac{c_{AZ}V_{IFS}}{c_{INT}V_{BFS}}\right\} - 1\right]^{-1}$$

Once again, the effect of this at the input is multiplied by the ratio of total input integrate times, so that, under equilibrium conditions,

$$c_{INres} = \pm\frac{V_{IFS}}{V_{BFS}}\left(1 + \frac{c_{DE}}{c_{INT}}\right)\left(c_X + c_D\right)\left[\exp\left\{\frac{c_{AZ}\,V_{IFS}}{c_{INT}V_{BFS}}\right\} - 1\right]^{-1} \tag{A7}$$

Those expert at skipping to the end of the difficult bit will recognize that as the final equation, in terms of complexity. So let us now see what it means. Clearly, the error term is greater, the larger $\frac{c_{DE}}{c_{INT}}$, and the smaller $\frac{c_{AZ}}{c_{INT}}$. For the ICL7104 combinations, (and also the ICL7103, and the data sheet systems for the ICL8053 pairs), these are both worst case near full scale input, where $\frac{c_{DE}}{c_{INT}} \approx 2$ and $\frac{c_{AZ}}{c_{INT}} \approx 1$. (Note that the minimum auto-zero time technique of section 4B will make $\frac{c_{AZ}}{c_{INT}} = 1$ for all input values). Substituting these, we find the worst case

$$c_{INres} \simeq \pm\frac{V_{IFS}}{V_{BFS}}\,(3)\left(c_X + c_D\right)\left[\exp\left(\frac{V_{IFS}}{V_{BFS}}\right) - 1\right]^{-1} \tag{A8}$$

Recall the c_D is fixed; and c_X must be between 0 and 1. The expression is now a function purely of the ratio of integrator and buffer full scale swings; the relationship is plotted in Figure A5, and shows the desirability of keeping the integrator swing higher than the buffer swing. Note also that the comparator delay (c_D in equation (A8)) is also effectively enhanced. This has the effect of shrinking the zero somewhat more than normally occurs. Since this term changes sign with polarity, the converter will have a tendency to keep the current sign at zero input.

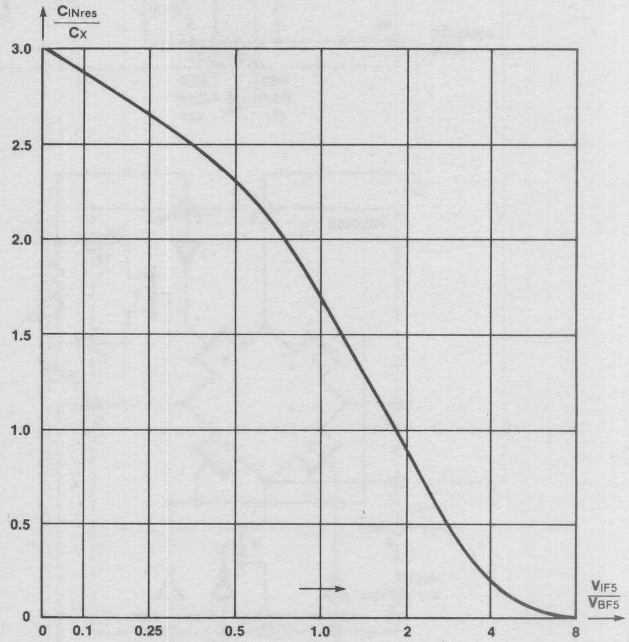

Figure A5: Auto-Zero Loop Residual vs. Integrator/Buffer Swing Ratio

The effects of noise should be mentioned here. The worst case value of residual shown in Figure A5 assumes a very gradual approach to equilibrium, and any noise spike causing the reading to flash to the next value will destroy all this carefully established residual value! Thus for any system with noise of ~ 1/3 count or more, the effect is greatly reduced, and even 1/10 count of noise will restrict the actual hysteresis value found in practice. The detailed analysis of the auto-zero residual problem in the presence of appreciable noise is left as an exercise for the masochist.

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